



Samsung NAND Flash Memory

**Memory Product &
Technology Division**

2000.3.15

NAND Flash Memory

Technology for Mass-Storage

- **Non-volatile and Low Power Operation**
- **Lowest Bit Cost Solid-State Memory**

Various Flash Memory Technologies

Technology	<i>NOR</i>	<i>DINOR</i>	<i>T-Poly</i>	<i>AND</i>	<i>NAND</i>
Structure					
Program Method	CHE	F-N	CHE	F-N	F-N
Erase Method	F-N	F-N	F-N	F-N	F-N
Layers	2P2M	3P2M	3P1M	3P2M	2P1M
Company	Intel, AMD	Mitsubishi	SanDisk	Hitachi	Samsung Toshiba

Reference : ISSCC 94, 95, 96 Flash Session

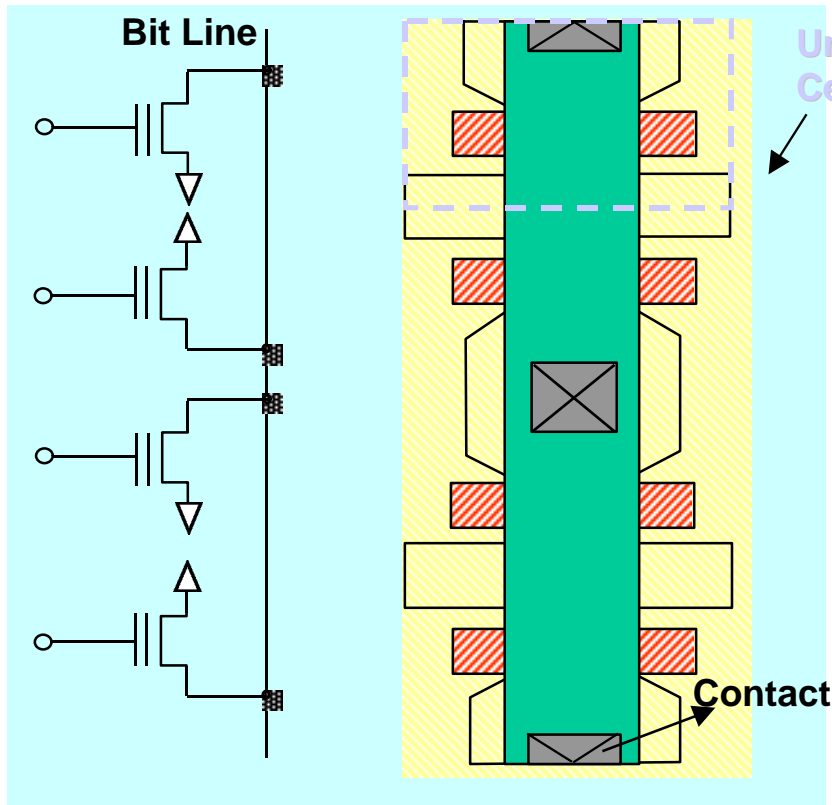
Unit Cell Comparison

Item	NOR TYPE	NAND TYPE
Vertical View		
Features	<ul style="list-style-type: none"> • One Tr. NMOS Floating Gate Device • Program : Hot - Electron • Erase : F-N Tunneling (BTBT Effect) 	<ul style="list-style-type: none"> • One Tr. NMOS Floating Gate Device • Program : F-N Tunneling • Erase : F-N Tunneling (No BTBT) • Low Vcc Possible

Cell Architecture Comparison

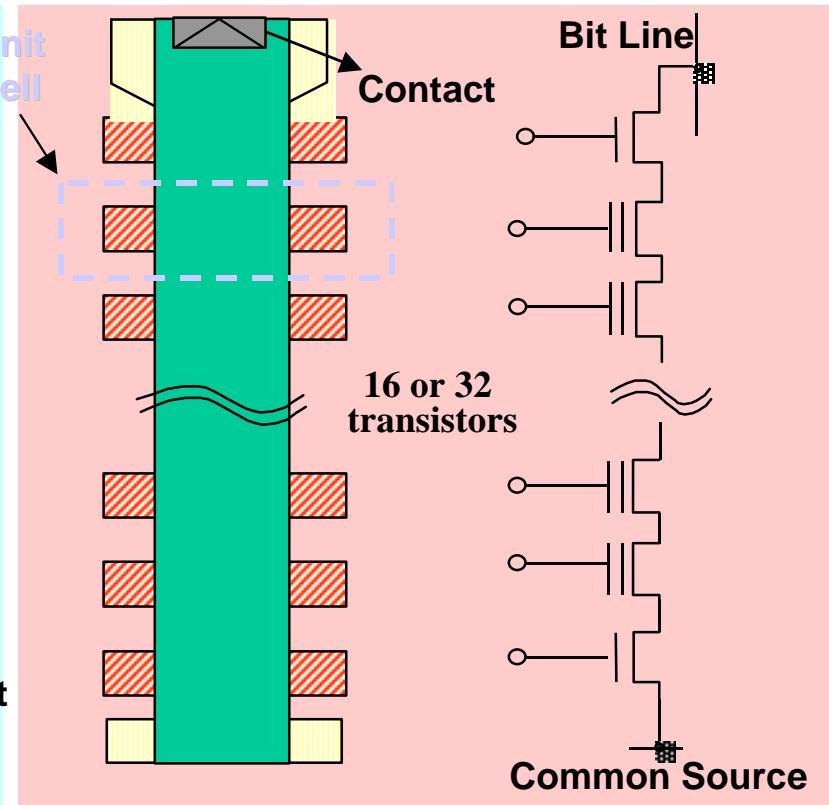
NOR TYPE

- Large cell and fast random access



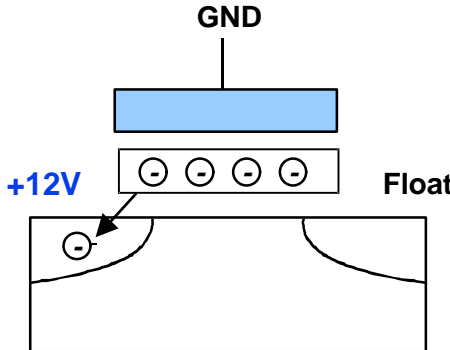
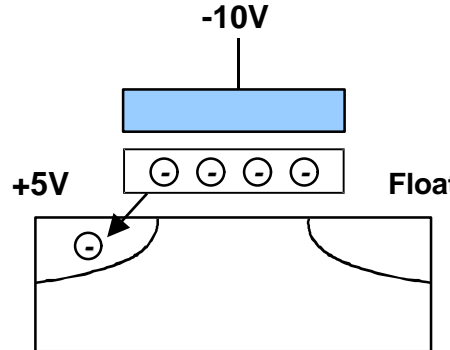
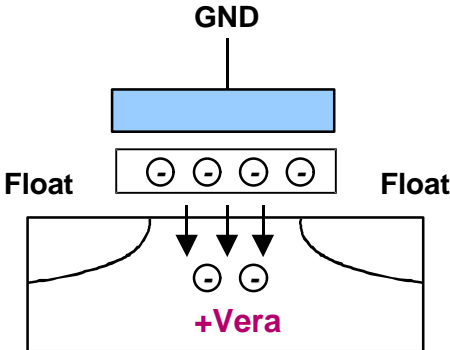
NAND TYPE

- Small cell, but fast sequential access



- Contact is the limiting factor for scale-down.
- Easy to Scale Down.

NOR Flash Erase Method

High Voltage Source Erase	Negative Gate Source Erase	Channel Erase
		
<p>Key Factors : Device Scalability , Voltage Scalability (Vcc, Charge Pump), Maximum High Voltage, Current Consumption(BTBT), Reliability(P/E Endurance, Retention)</p>		

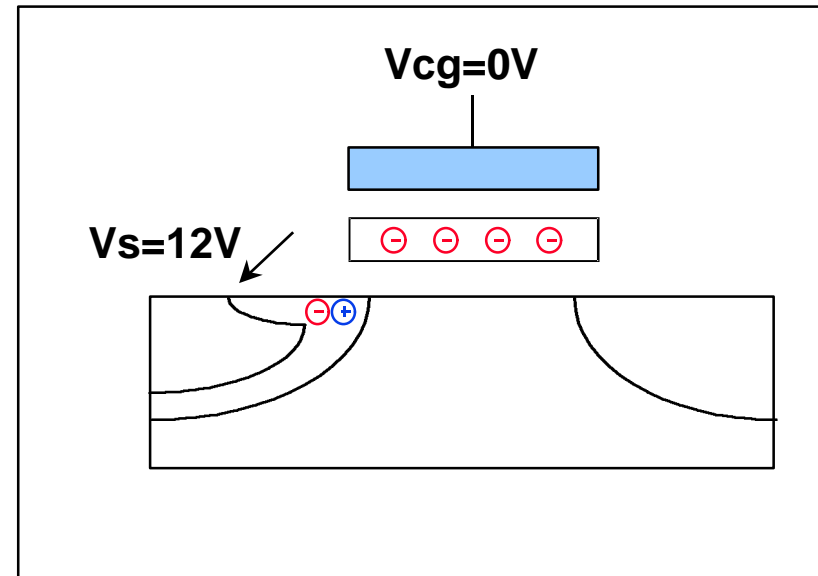
Reference :

1. K. Yoshikawa.. "Comparison of Current Flash EEPROM Erasing Methods .. " IEDM, pp.595-598, 1992.
2. K. Tamer San .. "Effects of Erase Source Bias on Flash EPROM Device Reliability," IEEE Trans. ED, vol.42, no. 1, pp.150-159, Jan. 1995.

BTBT (Band To Band Tunneling) Effect

- During Erase Operation
- Gate Potential Assisted BTBT Phenomena
- Increased V_s Current
- Reliability Issues due to Hot-hole Trapping

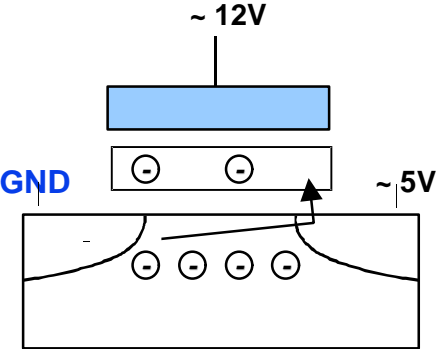
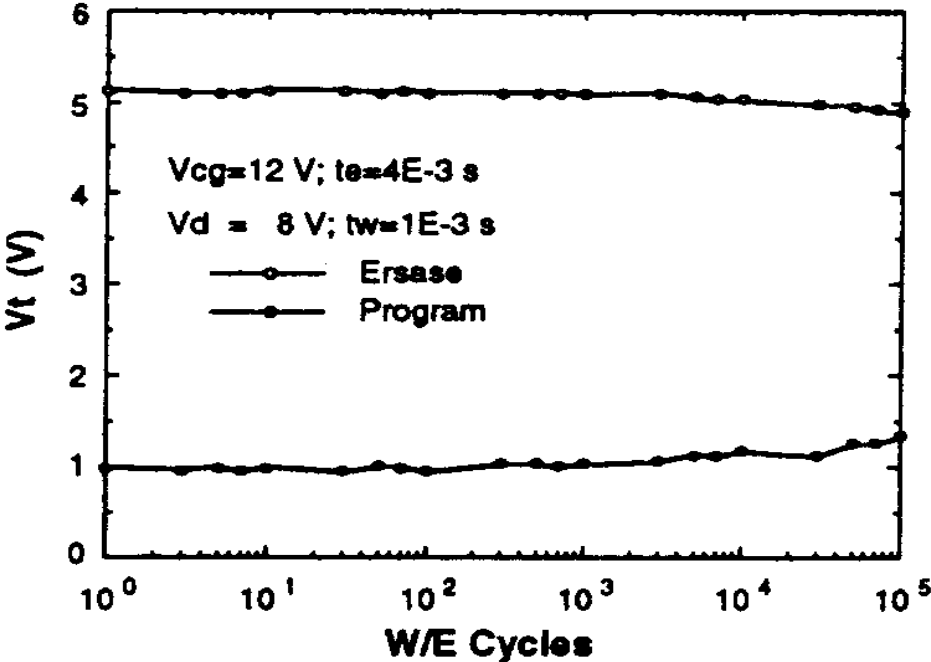
--> DD Structure for Source



■ References :

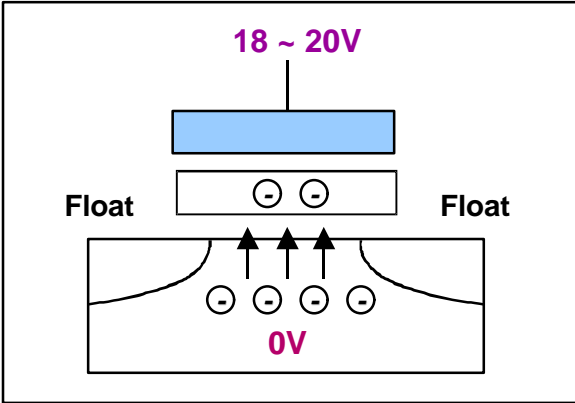
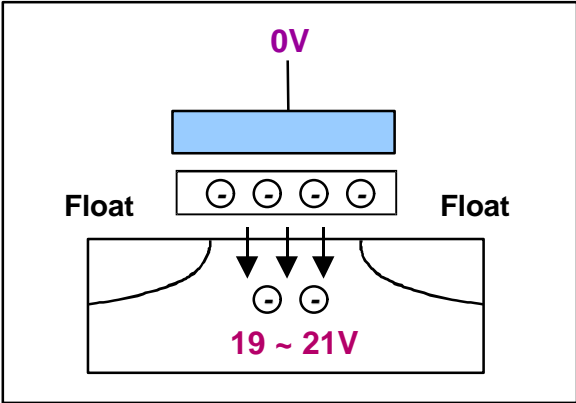
1. S. Haddad.. "Degradation Due to Hole Trapping in Flash Memory Cells," IEEE ED Letters, vol.10, no. 3, pp.117-119, March, 1989.
2. S. Keeny .."Complete Transient Simulation of Flash EEPROM Devices," IEEE Trans. ED, vol. 39, no. 12, pp.2750-2757, Dec. 1992.

NOR Flash Program Method & Endurance

Program Method	Typical Endurance Characteristics																					
 <p>The diagram illustrates the program method for NOR Flash. It shows a cross-section of a memory cell with a bit line on top and word lines on the side. The bit line is connected to a voltage source labeled $\sim 12V$. The word lines are connected to a voltage source labeled $\sim 5V$. The bit line is also connected to GND. The word lines are connected to GND. The diagram shows the bit line and word lines intersecting to form a memory cell.</p>	 <p>The graph shows the typical endurance characteristics of NOR Flash. The y-axis is V_t (V) ranging from 0 to 6. The x-axis is W/E Cycles on a logarithmic scale from 10^0 to 10^5. Two data series are shown: Erase (open circles) and Program (filled circles). The Erase series starts at $V_t \approx 1.0$ V and remains relatively constant. The Program series starts at $V_t \approx 5.2$ V and remains relatively constant. The test conditions are $V_{cg} = 12$ V; $t_a = 4E-3$ s and $V_d = 8$ V; $t_w = 1E-3$ s.</p> <table border="1"><thead><tr><th>W/E Cycles</th><th>Erase V_t (V)</th><th>Program V_t (V)</th></tr></thead><tbody><tr><td>10^0</td><td>1.0</td><td>5.2</td></tr><tr><td>10^1</td><td>1.0</td><td>5.2</td></tr><tr><td>10^2</td><td>1.0</td><td>5.2</td></tr><tr><td>10^3</td><td>1.0</td><td>5.2</td></tr><tr><td>10^4</td><td>1.0</td><td>5.2</td></tr><tr><td>10^5</td><td>1.0</td><td>5.2</td></tr></tbody></table>	W/E Cycles	Erase V_t (V)	Program V_t (V)	10^0	1.0	5.2	10^1	1.0	5.2	10^2	1.0	5.2	10^3	1.0	5.2	10^4	1.0	5.2	10^5	1.0	5.2
W/E Cycles	Erase V_t (V)	Program V_t (V)																				
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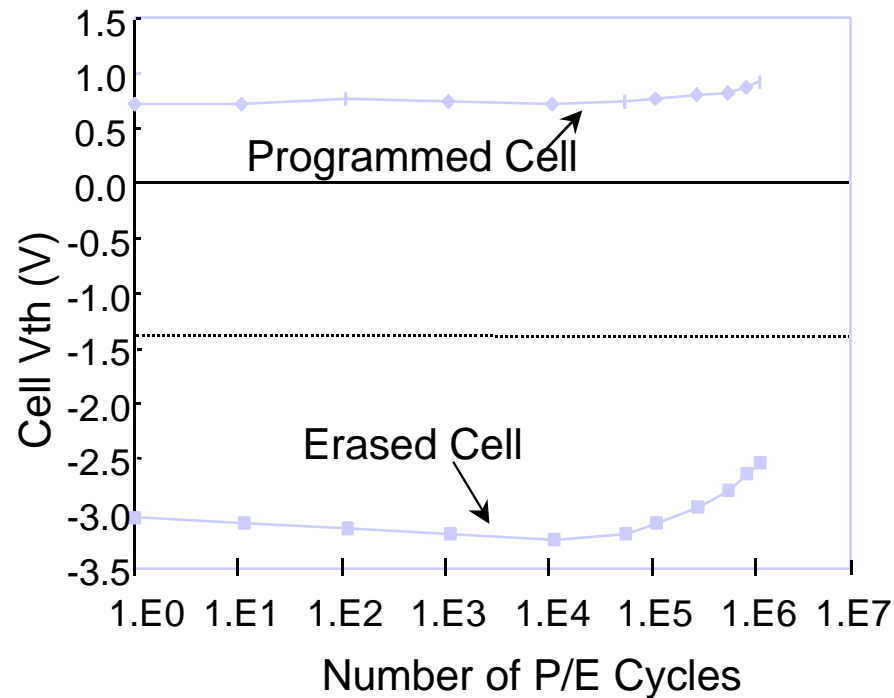
- **Hot Electron Injection**
- **Advantages**
 - . Fast Program Speed ($\sim \mu s$)
- **Disadvantages**
 - . Large Program Current ($\sim 500\mu A/cell$)
 - . Difficult Voltage Scaling
 - . Strong Charge Pump Circuit for Low V_{cc}

NAND Flash Program/ Erase Method

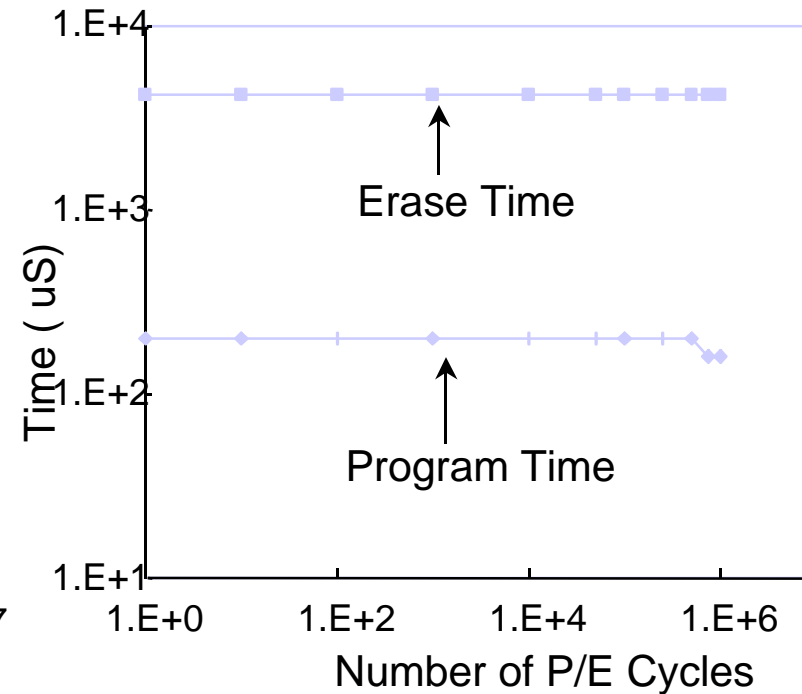
Program	Erase
	
<ul style="list-style-type: none"> ● Use F-N Tunneling ● Channel Inversion 	<ul style="list-style-type: none"> ● Use F-N Tunneling ● Channel Accumulation
<p>-> No DD Source (Easy Device Scaling) -> No BTBT Current (Easy Voltage Scaling)</p>	

NAND Flash Endurance vs. Characteristics

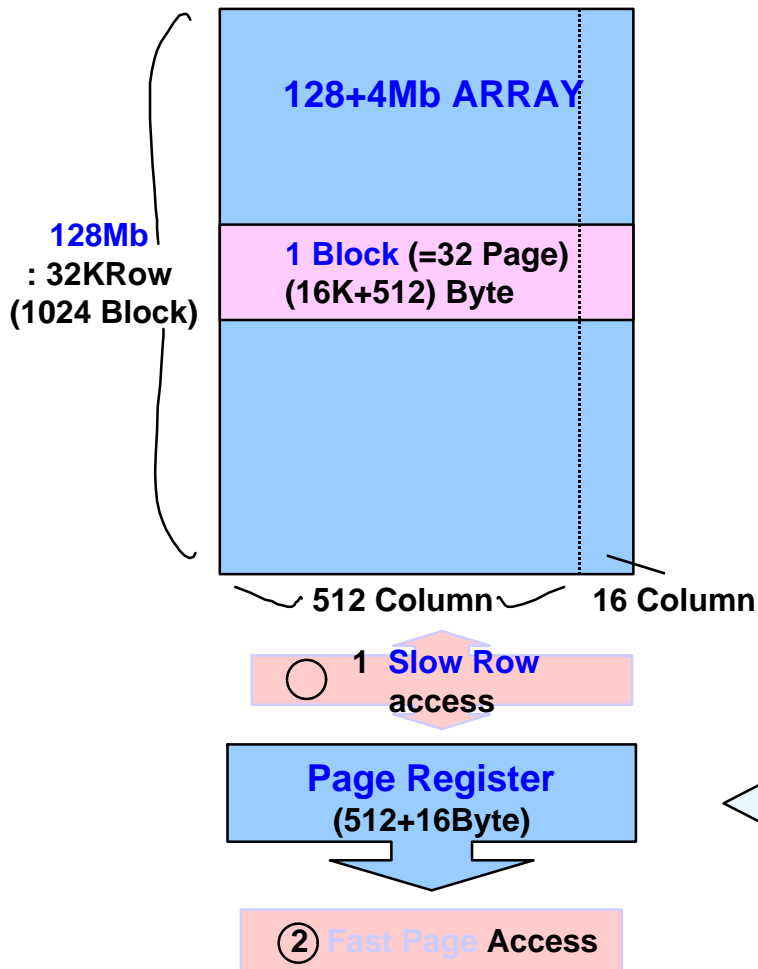
Cell Vth Shift



Program/ Erase Time Variation



NAND Flash Operation

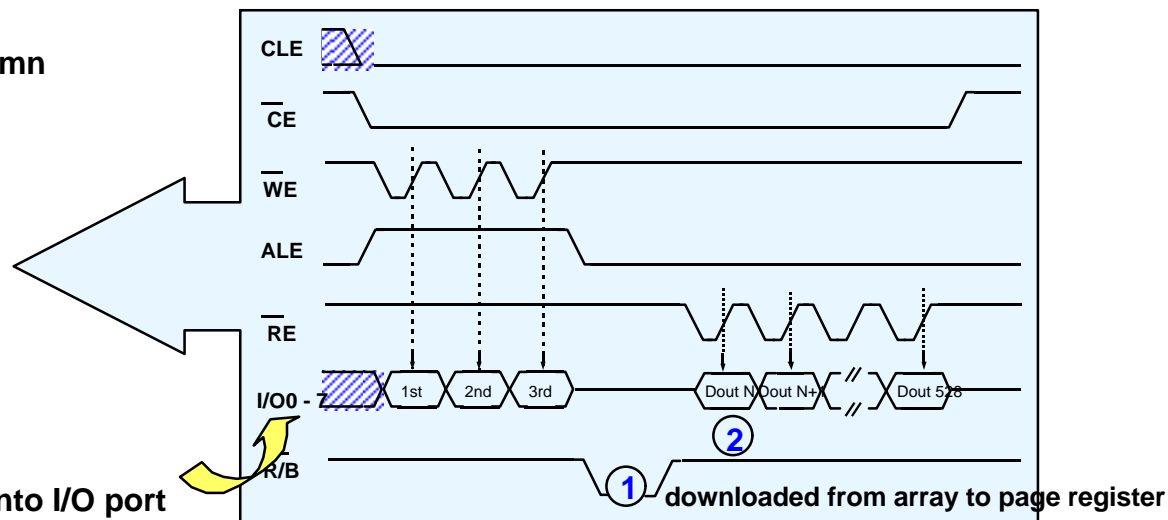


• Address map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1'st cycle	A0	A1	A2	A3	A4	A5	A6	A7
2'nd cycle	A9	A10	A11	A12	A13	A14	A15	A16
3'rd cycle	A17	A18	A19	A20	A21	A22	A23	*X

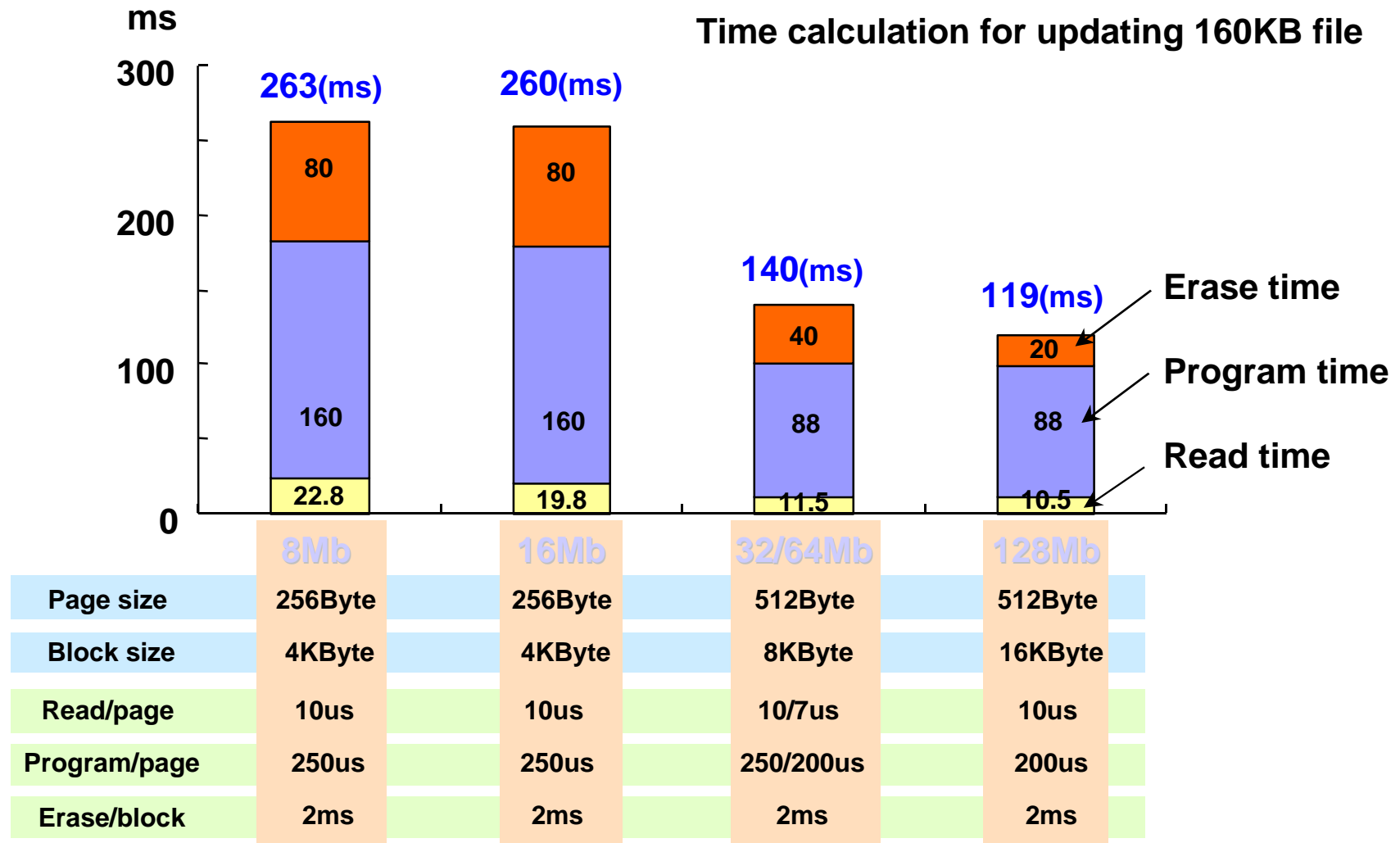
A0 ~ A7 : Selects the starting address of the 1st half of the register
 A9 ~ A13 : Selects 1 page of 1 block (32 pages)
 A14 ~ A23 : Selects 1 of 1024 blocks

• Read Operation

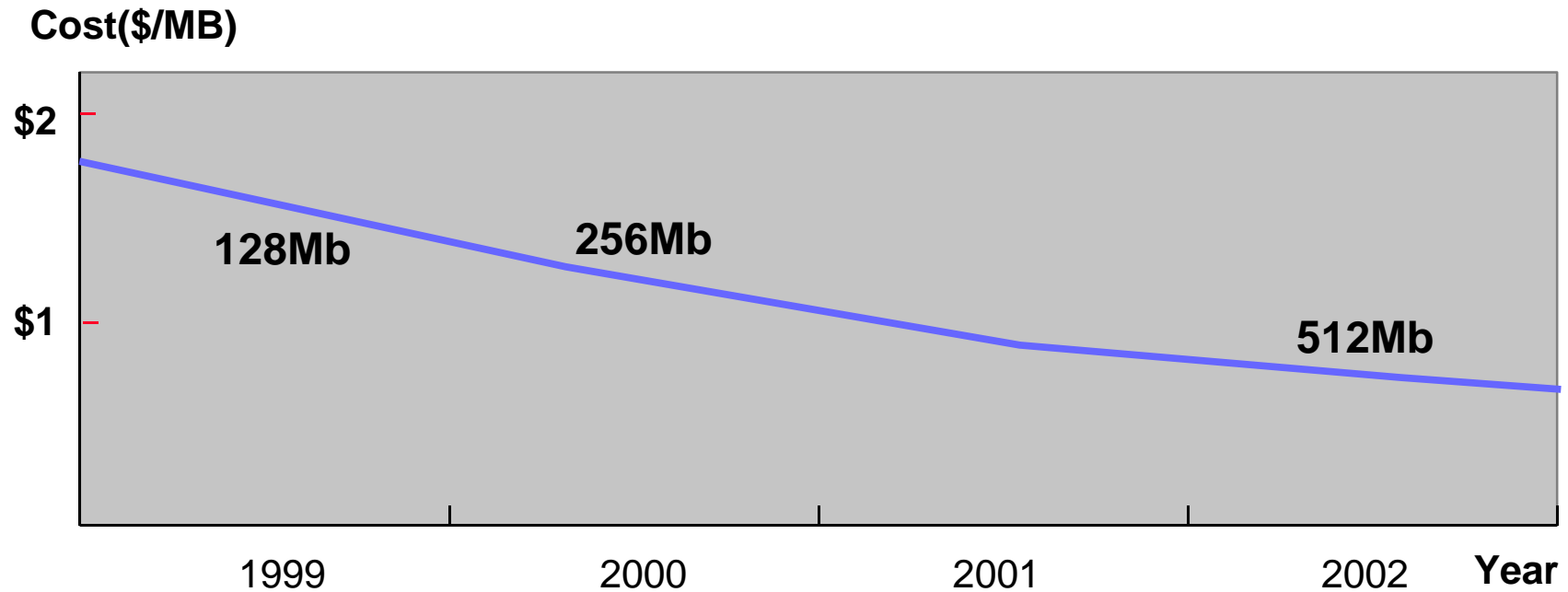


Command, address and data multiplexed into I/O port

NAND Flash Performance Analysis



Bit Cost Forecast of NAND Flash



- Bit cost continues to be dropped as the memory density grows.

Flash Memory Application Segment

Applications	Chip Storage (Mbit)									Key Features
	1	2	4	8	16	32	64	128	256	
EPROM Replacement <ul style="list-style-type: none"> - PC BIOS Firmware - OS/APPS Software - D.Cellular Phone - Boot Code Storage 										Random Access <ul style="list-style-type: none"> - Separate Add./Data Line - Chip or Large Erase Block - 1 piece/system
Mass Storage <ul style="list-style-type: none"> - PCMCIA ATA Card - Solid-State Disk - Digital Still Camera - Digital Audio Recorder - Music Player 										Low Cost <ul style="list-style-type: none"> - High Speed Sequential Access - Mid./Small Block Size - Single Voltage(3V)