

# ***Alternatives to Using NAND Flash White Paper***

Ziv Paz

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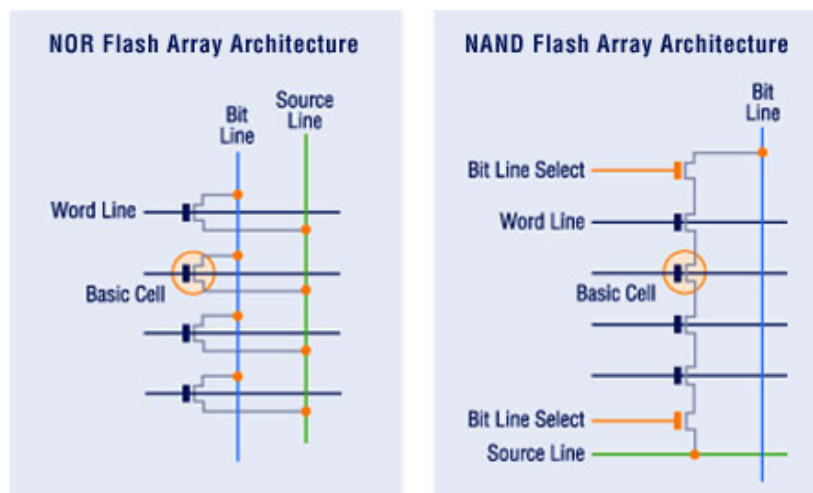
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## INTRODUCTION

The popularity of feature phones, camera phones, MP3 players, video-on-demand, and other new applications is on the rise. In a saturated handset market, handset vendors are pushed by the carrier's desire to increase ARPU and by their own need to drive users to upgrade their handsets. As a result, all handset manufacturers carry new data-centric devices offering rich multimedia and productivity features aimed at savvy business customers and the "trendy" teenager segment. Many of these devices have complex operating systems, large suites of applications and a large amount of memory for user data. More and more, this memory is NAND flash-based as opposed to NOR flash-based. But among the NAND solutions, there are many implementation alternatives offering different merits and challenges.

## WHY NAND IS BECOMING A MUST IN MOBILE PHONES

Two main technologies (Figure 1) dominate the non-volatile flash memory market today: NOR and NAND. Until recently hardware engineers were unfamiliar with the differences between the architectures of these two technologies, but this is no longer the case.



*Figure 1: Comparing NOR and NAND Flash Architectures*

While NOR offers eXecute In Place (XIP) capabilities and high read performance, it is expensive per MB, thus mostly cost-effective in low capacities (1MB-4MB). Another disadvantage of NOR is its extremely low write and erase performance. NAND architecture, on the other hand, offers high cell densities and high capacity, combined with fast write and erase rates. But since it is accessed in blocks of 512MByte (called pages) it cannot be used for XIP, has inherent bad blocks and is prone to low reliability due to random errors generated by physical effects in the geometry of the NAND gates.

There are many other differences between these two technologies that will not be covered by this article, but the technical characteristics strongly differentiate the types of applications using them. NOR is typically used for executing small amounts of code, mainly in capacities up to

4MB, and is common in applications such as simple consumer appliances, low-end cell phones, and embedded applications. Raw NAND is mainly used for data storage in applications such as memory cards and MP3 players.

Since NAND flash does not have a standard memory interface and because it requires extensive handling to prevent errors in the stored data, it requires an additional controller (as in the case of removable memory cards).

From 16MB and upwards, NOR flash loses its cost-effectiveness. Furthermore, its sluggish write speed and very slow erase time do not provide suitable performance for a data storage device.

Due to the high densities of NAND flash and the better cost per Megabyte, NAND is by far the best media for data storage. However, NAND technology has some inherent limitations that must be dealt with to insure reliability of the data stored and of the overall system/handset. The next section examines these limitations and describes NAND alternatives for today's terminals.

## USING NAND IN A DESIGN

One of the main considerations of working with a flash media is its reliability. Flash is the preferred storage solution for systems in need of a very long life span, and huge MTBF rates (military applications, consumer appliances, mobile devices, communications and many more). When looking at the reliability of NAND, three main factors must be taken into account:

- Bit-flipping
- Bad block handling
- Life span (number of erase cycles allowed).

### Bit-Flipping

All flash architectures today suffer from a phenomenon known as “bit-flipping”. On some occasions (usually rare, yet more common in NAND than in NOR), a bit is either reversed, or is reported reversed. Although a single reversal may seem insignificant, this “minor” glitch may hang your system completely if it corrupts a critical file. When the problem is just of reporting, repeating the read operation may solve it; however, if the bit was actually reversed, an error detection/correction algorithm must be applied (as offered in the DiskOnChip®). Since this phenomenon is more common in NAND devices, all NAND vendors recommend using an EDC/ECC algorithm. When using NAND for multimedia information, this problem is not critical, but when using it as a local storage device to store the system OS, configuration files and other sensitive information, an EDC/ECC system MUST be implemented.

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## Bad Block Handling

Due to yield considerations, NAND devices are shipped with bad blocks randomly scattered throughout the media. Shipping NAND devices free of bad blocks comes with a very high price tag caused by the low production yield rate, and is therefore not a cost-effective option.

Working with NAND devices, especially for local storage, requires initially scanning the media for bad blocks, and then mapping them all out so they are never used. Failing to do so in a reliable manner may result in a high failure rate of the final device, and even device recall.

## Life Span/Endurance

As mentioned above, a flash block must be erased before writing to it. But the number of times that it can be erased is limited. NAND devices offer up to 10 times the life span of NOR devices. In fact, since the block size of a NAND device is usually about eight times smaller than that of a NOR device, each NOR block will be erased relatively more times over a given period of time (especially significant when working with small files) than each NAND block. This further extends the gap in favor of NAND.

Endurance and reliability are closely linked. When reaching the maximum allowed erase cycles, the reliability of the flash deteriorates dramatically. Therefore, maximizing the endurance of the flash has a positive effect not only on the “life” of the flash but also on the “quality of life” of the flash.

## Ease of Use

Using a NOR-based flash is a straightforward process. Just connect it as you would connect other memory devices, and run your code directly from it (if you don’t mind the slow performance). Using NAND, on the other hand, is a tricky issue. NAND has an I/O interface and requires toggling two signals (OLE and CLE). Accessing one NAND from vendor A is not necessarily the same as accessing another NAND from vendor B. A driver **MUST** be written and used for performing any operation on a NAND device. Writing information to NAND is also tricky since you have to make sure you are not writing the information to a bad block. This means that virtual mapping **MUST** be implemented on NAND device at all times.

## Software Support

A distinction must be made between two levels of software support: basic read/write/erase operations, and high level software for disk emulation and flash management algorithms (including wear leveling, performance optimizations, etc.).

Running code from NOR devices requires no special software support. Running code from NAND requires a driver, usually referred to as an MTD (memory technology driver). Both NAND and NOR require MTDs for write and erase operations. While MTDs are basically all that is required for NOR write/erase, a NAND driver must also have bit error and bad block management code.

Higher-level software is available for NOR devices from many vendors, yet the standard is M-Systems' NOR version of its TrueFFS® drivers, used by Wind River, Microsoft, QNX, Symbian, and even licensed by Intel. Other software packages are available by other third party software houses. NAND devices, on the other hand, lack noticeable software support. However, its high capacity, low cost and fast performance make NAND an ideal candidate for data storage in general, and hard drive emulation (block management) specifically. Based on NAND technology, M-Systems' DiskOnChip is supported by TrueFFS for both disk emulation and for NAND flash management, including bit error correction, bad block handling, and wear leveling, thus conveying all of NAND advantages without any of the disadvantages of difficult system integration. TrueFFS is provided both as source code and in binary format for all major operating systems such as VxWorks, Windows CE, Linux, QNX/Neutrino, Windows XP/XP Embedded, Windows NT/NT Embedded, DOS and many more.

## Booting from NAND

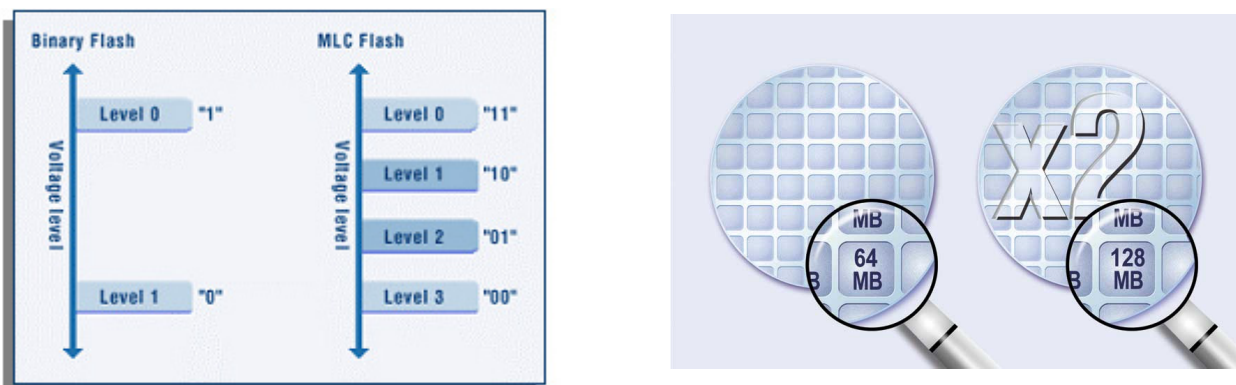
Since NAND is not a random access device, it has no XIP functionality. However, there is a strong incentive to enable boot from NAND to achieve greater cost savings by enabling the designer to eliminate expensive NOR flash from the platform.

To allow booting from NAND, the designer must utilize a very small XIP device, containing system initialization code and some code used to shadow the main boot code and OS image from the NAND media into the host RAM and execute from there.

This is further complicated by two conflicting requirements: performance and reliability. Copying the boot code and the OS image from NAND to the system RAM is a time-consuming task that affects the boot time of the device. But higher performance cannot be provided at the expense of reliability, since an error in copying boot code from the NAND to the system RAM will very likely make the platform inoperative.

## MULTI- LEVEL CELL (MLC) NAND

One of the recent developments in NAND technology is the introduction of MLC NAND by Toshiba. MLC NAND allows a 2-bit representation on a single physical cell, increasing the flash density by a factor of 2, as shown in Figure 2.



*Figure 2: Compared with Binary NAND, MLC NAND Doubles Flash Density*

While MLC NAND represents a breakthrough in cost structure, the major, inherent limitations of the technology – substantially slower performance, and problematic reliability – are making it hard and tedious to integrate into real life applications.

DiskOnChip G3 family addresses these issues. Based on Toshiba's MLC NAND and M-Systems' x2 technology, it offers a fast, reliable and cost-effective MLC NAND-based product.

This is achieved by:

- **Perfecting reliability** - x2 technology implements an advanced error detection and correction mechanism, based on a combination of cutting-edge algorithms. The result is a perfect device (absolute data and code reliability throughout entire device life span).
- **Enhancing performance** - x2 technology implements parallel multi-plane operations, provides DMA support and a configurable burst mode, all aimed at delivering exceptional write, read and erase performance.

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## NAND DESIGN OPTIONS

### Raw NAND (GPIOs and Software)

Although highly *not* recommended, it is feasible to manage NAND flash by means of software alone. This can be done by programming the general purpose I/Os in the processor (assuming such signal are available) to act according to the NAND interface, by implementing the error detection algorithms and error correction algorithms in software and by implementing an efficient flash translation layer to provide bad block management, wear leveling, dynamic mapping and other managerial tasks.

The software overhead of such an implementation results in very low performance, mostly due to the heavy error detection code required for every read/write to the flash.

### NAND with External Controller

NAND can be used in conjunction with a specialized companion controller so that it can be connected to the host standard memory bus, where NOR and SRAM usually reside. It may also include an implementation of an error detection algorithm to enhance performance and reduce the software overhead.

The main benefit of such a solution is the fact that a fairly simple controller can be designed specifically to support different NAND flash solutions. However, this is a relatively costly approach, both in dollars and in size. A NAND controller may use 6x6mm to 10x10mm of precious PCB space, in addition to the space occupied by the NAND media.

But such a solution may leave the developer without any clear point of contact for support, and the integration responsibility will fall on the designer's shoulders. Issues such as these will probably arise: Will the software to manage the NAND be procured from the NAND manufacturer or from the NAND controller vendor? Will the software manage flash from other flash vendors as well? If there is a bug in software or hardware, which vendor will resolve it: the flash vendor, the controller vendor or the host platform vendor?

### NAND with Chipset Controller

Due to the growing popularity of NAND, a number of mobile application processor vendors have attempted to provide out-of-the-box NAND support by embedding a controller inside their processors. While this is clearly an improvement over the previous alternatives, it is still lacking in its flexibility. During the lengthy design and market cycles that such a new application processor requires, NAND flash will have evolved. Therefore, the chipset will invariably support outdated flash devices instead of the current products on the market.

The market already shows evidence of this time gap. Recent major developments in NAND flash are not all supported by application processors, including 16-bit devices, different page sizes (an important factor when reading/writing to the flash) and usage of MLC technology.

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As in the previous implementation, it is not clear who will maintain the required software and provide ongoing support. This remains to be seen, since such application processors have just begun to enter the market.

Booting from NAND remains a major weakness to this approach, since none of the chipset implementations include error correction for the boot code stored in the NAND, which can result in fatal errors and even a system crash.

## DiskOnChip

DiskOnChip is a NAND-based device with a NOR interface, boot capabilities and TrueFFS complementary software, allowing easy device management under any operating system.

DiskOnChip is a monolithic device which implements the controller on the same silicon die as the flash array to maximize performance, reliability and cost structure.

TrueFFS software is closely integrated to work with DiskOnChip hardware, providing a balance between performance and ease-of-use. For example, the heavy error detection algorithms are implemented in hardware, while the lighter and less frequently used error correction algorithms are implemented in software.

With a NOR-like hardware interface, it is easy to connect DiskOnChip to any existing platform. The automatic download mechanism residing in the controller allows booting the system in a fast and reliable fashion.

DiskOnChip G3 is the newest member of the DiskOnChip product line. It enables the use of MLC NAND technology by elevating its performance and reliability of MLC NAND to the required levels. This is a monolithic design (single-die silicon) that internally uses two banks of MLC NAND to achieve high capacities, but as with all DiskOnChip solutions, the interface remains straightforward.

The hardware signals for DiskOnChip G3 and the previous DiskOnChip generation are backward compatible, enabling a developer to migrate from an existing DiskOnChip design to DiskOnChip G3 in easy steps. Additional value can be found in new performance-enhancing features such as the burst mode, DMA support and an interrupt handler, which were not part of the previous design. For more information please visit: [www.m-sys.com](http://www.m-sys.com) or [www.diskonchip.com](http://www.diskonchip.com).

## SUMMARY

The trend of using NAND in mobile platforms is pushed by new and growing data services offered by carriers, increasing the requirement for data storage, and by hardware manufacturers' desire to decrease BOM cost.

Solving the complicated issue of NAND flash management and providing full disk emulation and boot capabilities, DiskOnChip provides the most attractive solution in terms of performance, reliability, ease-of-integration and maturity. DiskOnChip can be used for both code and data storage, usually used in applications that require an operating system and a file system such as PDAs, feature phone, smartphones and converged devices.

## HOW TO CONTACT US

### USA

M-Systems Inc.  
8371 Central Ave, Suite A  
Newark CA 94560  
Phone: +1-510-494-2090  
Fax: +1-510-494-5545

### Japan

M-Systems Japan Inc.  
Asahi Seimei Gotanda Bldg., 3F  
5-25-16 Higashi-Gotanda  
Shinagawa-ku Tokyo, 141-0022  
Phone: +81-3-5423-8101  
Fax: +81-3-5423-8102

### Taiwan

M-Systems Asia Ltd.  
Room B, 13 F, No. 133 Sec. 3  
Min Sheng East Road  
Taipei, Taiwan  
R.O.C.  
Tel: +886-2-8770-6226  
Fax: +886-2-8770-6295

### China

M-Systems China Ltd.  
25A International Business Commercial Bldg.  
Nanhu Rd., Lou Hu District  
Shenzhen, China 518001  
Phone: +86-755-2519-4732  
Fax: +86-755-2519-4729

### Europe

M-Systems Ltd.  
7 Atir Yeda St.  
Kfar Saba 44425, Israel  
Tel: +972-9-764-5000  
Fax: +972-3-548-8666

### Internet

<http://www.m-sys.com>

### General Information

[info@m-sys.com](mailto:info@m-sys.com)

### Sales and Technical Information

[techsupport@m-sys.com](mailto:techsupport@m-sys.com)

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